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Tri-State DC-DC Buck Converter with Efficient Conversion Ratio

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Abstract

In modern electronic applications the requirement of step down dc-dc conversion is much more. To estimate this process this dc-dc buck converter is implemented with perfect duty cycles as a proposed work. The converter comprises symmetrical half bridges and its structures. The voltage differences across two bridges has been examined in presented and balanced condition of operation is achieved. Then a modulation strategy which can satisfy the operation of the converter is proposed with the capacitor voltages self balance, and the function of the output dc voltage Vo is deduced.

Keywords: DC-DC buck converter, High step-down conversion, Non-extreme duty cycles, Three-level

Introduction

The **Ćuk converter** (pronounced *Chook*, sometimes incorrectly spelled **Cuk**, **Čuk** or **Cúk**) is a type of DC-DC converter that has an output voltage magnitude that is either greater than or less than the input voltage magnitude. The non-isolated Ćuk converter can only have opposite polarity between input and output. It uses capacitor as its main energy-storage component, unlike most other types of converters which use an inductor. It is named after Slobodan Ćuk of the California Institute of Technology, who first presented the design.

Non-isolated Ćuk Converter

A non-isolated Ćuk converter comprises two inductors, two capacitors, a switch (usually a transistor), and a diode. Its schematic can be seen in figure 1. It is an inverting converter, so the output voltage is negative with respect to the input voltage.

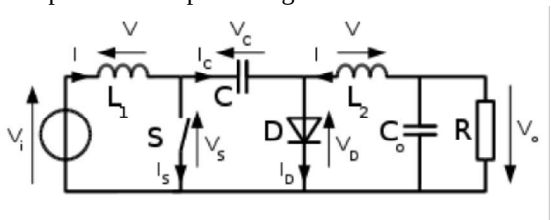

Fig 1: Schematic of a non-isolated Ćuk converter.

The capacitor C is used to transfer energy and is connected alternately to the input and to the output of the converter *via* the commutation of the transistor and the diode (see figures 2 and 3).

During the subinterval where the converter behaves like a PWM boost converter in the charging and transferring modes, all of the auxiliary components are inactive. Therefore, there is no additional loss in these states. In order to explain the operation of the converter and to quantify its behavior, the following conditions are assumed: The two inductors L1 and L2 are used to convert respectively the input voltage source (Vi) and the output voltage source (Co) into current sources. Indeed, at a short time scale an inductor can be considered as a current source as it maintains a constant current.

This conversion is necessary because if the capacitor were connected directly to the voltage source, the current would be limited only by (parasitic) The converter operation and design procedure based on the steady-state are analyzed in the next section.

The elimination of the turn-off switching losses is explained in Section IV. In section V the current control strategy is introduced. The design procedure is discussed in Section VI. The simulation and experimental results from a 250 W, 400 Vdc prototype converter at 100 kHz for universal input voltage (90-264 Vrms) applications are given in Section VII and VIII, respectively.

These results verify the feasibility of the design process and the advantages of the proposed topology. The proposed converter is suitable for single-phase, power factor correction and universal input voltage applications where high efficiency and low EMI (Electro Magnetic Interference) are important.

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The proposed converter consists of an auxiliary circuit which can provide the ZVS condition for the main switches if it is controlled properly. Conventional ZVS topologies reduce the turn-on switching losses, but the proposed topology reduces the overlap between the voltage and the current on the power switches both during switch turn-off and turn-on (section IV). Therefore, bridgeless PFC and the ZVS technique reduce conduction losses and switching losses, respectively. This maximizes the efficiency and consequently the limitation on switching frequency can be eliminated.

To provide soft switching for the main power switches at turn-on, the auxiliary switch is turned on for a fixed period of time. This provides the soft switching condition for the main switches and reduces the overlap between the current and the voltage at switching times. The bridgeless PFC operation is symmetrical in the two under the three symmetrical solutions under.

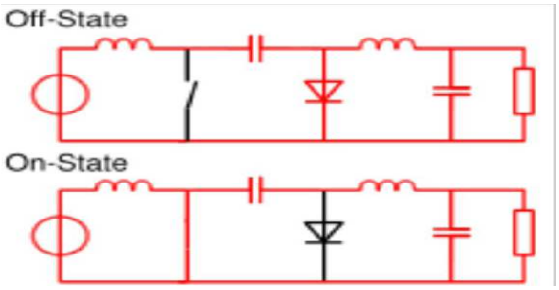

Fig 2: The two operating states of a non-isolated Ćuk converter.

resistance, resulting in high energy loss. Charging a capacitor with a current source (the inductor) prevents resistive current limiting and its associated energy loss. As with other converters (buck converter, boost converter, buck-boost converter) the Ćuk converter can either operate in continuous or discontinuous current mode. However, unlike these converters, it can also operate in discontinuous voltage mode (i.e., the voltage across the capacitor drops to zero during the commutation cycle).

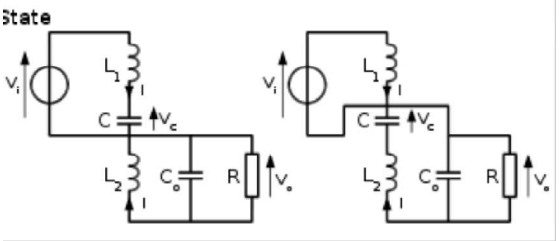

Fig 3: The two operating states of a non-isolated Ćuk converter.

In this figure, the diode and the switch are either replaced by a short circuit when they are on or by an open circuit when they are off. It can be seen that when in the Off state, the capacitor C is being charged by the input source through the inductor L1. When in the On state, the capacitor C transfers the energy to the output capacitor through the inductance L2.

Continuous Mode

In steady state, the energy stored in the inductors has to remain the same at the beginning and at the end of a commutation cycle. The energy in an inductor is given by:

$$E = \frac{1}{2} L I^2 \quad (1)$$

This implies that the current through the inductors has to be the same at the beginning and the end of the commutation cycle. As the evolution of the current through an inductor is related to the voltage across it:

$$V_L = L\frac{dI}{dt} \quad (2)$$

it can be seen that the average value of the inductor voltages over a commutation period have to be zero to satisfy the steady-state requirements. If we consider that the capacitors C and Co are large enough for the voltage ripple across them to be negligible, the inductor voltages become: in the off-state, inductor L1 is connected in series with Vi and C (see figure 2). Therefore $VL1 = Vi - VC$. As the diode D is forward biased (we consider zero voltage drop), L2 is directly
connected to the output capacitor.

Therefore $VL2 = Vo$ in the on-state, inductor L1 is directly connected to the input source. Therefore $VL1 = Vi$. Inductor L2 is connected in series with C and the output capacitor, so $VL2 = Vo + VC$ The converter operates in on-state from t=0 to t=D·T (D is the duty cycle), and in off state from D·T to T (that is, during a period equal to (1-D)·T). The average values of VL1 and VL2 are therefore:

$$\bar{V}_{L1} = D \cdot V_i + (1-D) \cdot (V_i - V_C) = (V_i - (1-D) \cdot V_C) \quad (3)$$
$$\bar{V}_{L2} = D\,(V_o + V_C) + (1-D) \cdot V_o = (V_o + D \cdot V_C) \quad (4)$$

As both average voltage have to be zero to satisfy the steady-state conditions we can write, using the last equation:

$$V_C = -\frac{V_o}{D} \quad (5)$$

So the average voltage across L1 becomes:

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$$\bar{V}_{L1} = \left(V_i + (1-D)\cdot\frac{V_o}{D}\right) = 0 \qquad (6)$$

Which can be written as:

$$\frac{V_o}{V_i} = -\frac{D}{1-D} \qquad (7)$$

It can be seen that this relation is the same as that obtained for the Buck-boost converter.

Related Structures Inductor Coupling

Instead of using two discrete inductor components, many designers implement a *coupled inductor Ćuk converter*, using a single magnetic component that includes both inductors on the same core. The transformer action between the inductors inside that component gives a *coupled inductor Ćuk converter* lower output ripple than a Ćuk converter using two independent discrete inductor components.

Therefore, one half-cycle of the converter operation is explained here. The auxiliary circuit is divided into two symmetric sections too. Due to the input line half-cycles, one section is inactive. Thus another section of the proposed auxiliary circuit provides the soft switching condition for the main switches. Thus both sections have no effect on the converter efficiency when they are in the inactive mode. All components are ideal; the converter operates in the steady state at a fixed switching frequency (f_S). The input voltage (V_{in}) is a sine wave that is assumed to be constant (V_g) in a switching cycle. The output voltage (V_O) is also constant, and the switching frequency is much higher

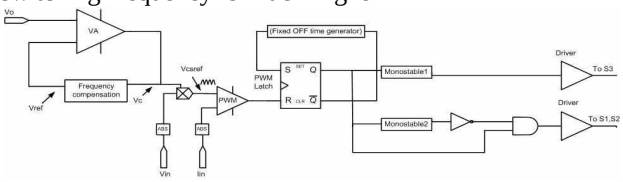

Fig.4. Auxiliary control circuits block diagram and controller

auxiliary circuit which provides soft switching for the main switches. C_{s1} and C_{s2} shown across S_1 and S_2 are the parasitic capacitance of the switches.

L_{r1} and L_{r2} provide soft switching for the main diodes (D_1, D_2) and reduce di/dt at turn-off times. Moreover, in conventional boost based PFC converters, conduction losses are higher when compared to diode rectifiers. To reduce conduction losses, the rectifier circuit and the PFC have been combined to introduce a bridgeless PFC converter. This combination decreases the conduction losses by reducing the number of semiconductor components in the line current path.

In bridgeless PFC, the body diode of S_2 conducts in the entire positive half line cycle and the body diode of S_1 conducts in the entire negative half line cycle. Using the ZVS technique for this converter can lead to even higher efficiencies. In this paper, a new ZVS PFC converter is proposed.

To clear the effect of the auxiliary circuit on the main switches, at first, it has been implemented for one switch, as shows the waveforms of the voltage across the main switch S2 and the current through it at the turn-on and turn-off times. It is important to adjust the gate drive signals of the main and auxiliary switches exactly. The gate drive signal of the main and auxiliary switches.

The waveforms of the input voltage and current and the input line current harmonics of the ZVS-PWM bridgeless rectifier at the rated 250 W are shown in Fig. 20.Based on these waveforms, the current is practically sinusoidal with a low total harmonic distortion and a high power factor. It can be seen that the experimental results, shown in Fig. 20, are in good agreement with the theoretical analysis and the simulated results which have been the measured efficiencies of the different converters such as the proposed ZVS bridgeless PFC circuit.

The ZVS bridgeless PFC circuit with one switch in ZVS, the conventional boost ZVS converter and the hard-switching conventional boost converter.

Depending on the operating conditions, using the proposed converter can improve the efficiency in the range of 3% to 4.7%.

This converter has a higher efficiency when compared to its conventional PWM hard-switching counterpart, due to the soft switching and the lower conduction losses in the power flow path during rectification. This converter realizes soft switching for both the turn-off and turn on times. The overlap between current and voltage reduces through the main switches during the fall time.

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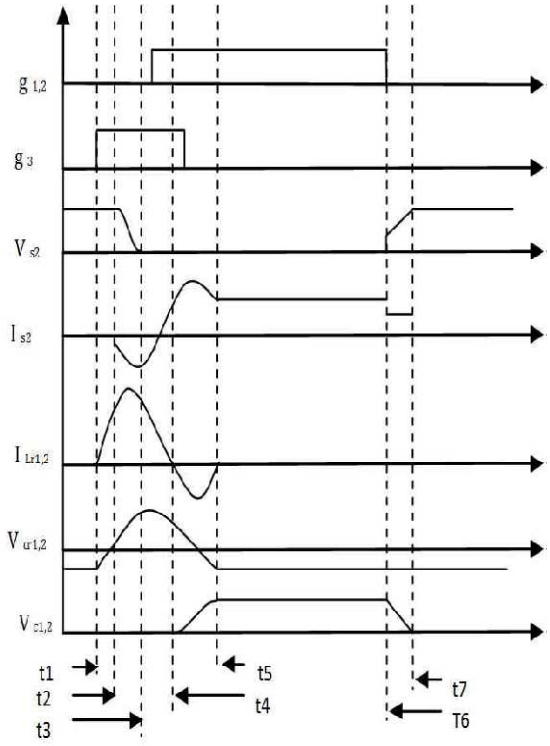

Fig. 5. Theoretical auxiliary circuit's waveforms during a switching period

Based on the converter analysis, characteristic curves have been obtained and a step-by-step design procedure for the converter has been introduced. Experimental results with a 250 W prototype at 100 kHz, verify the feasibility and advantages of the introduced topology. Based on the given approach, the converter prototype has been designed, and simulation and experimental results have been presented. An efficiency of 94.7% is achieved which improves the efficiency more than 4.7%, when compared to the hard-switching converter.

For low and medium voltage DC loads requirements, buck switch-mode rectifiers have been proposed to step-down the output voltage. However, these converters are not suitable for step-up voltage conversions. To produce a high DC voltage, boost rectifiers have been proposed in. Due to inductors placed in series with the inputs, boost converters draw a continuous current flow and contain a low switching frequency content.

These features give boost converters an advantage over current-source buck converters, which draw pulse width modulated currents. However, recent technological developments require power supplies with wider conversion rates especially in photovoltaic applications and electric vehicle technologies.

As a result, major deterioration of the output voltage and inductor current signals occur. Another approach is the use of transformers to step-up/down the DC output. However, limited power capacity, design complexity, poor cross regulation, and high inrush currents are some of the drawbacks of using a transformer.

Progress in digital technologies such as field programmable gate arrays (FPGAs) has enabled engineers to develop complex controllers without considerable hardware modifications. The integration of software and a FPGA for real-time simulation has been done in.

Hardware-in-the-loop simulation is a tool for the implementation and verification of a controller's functionality without increasing the risk of damaging the prototype during actual testing. Moreover, conventional simulations do not consider the resolution limit of the processor chip.

By implementing a simulation accuracy, the controller design can be tested under realistic conditions. For low and medium voltage DC loads requirements, buck switch-mode rectifiers have been proposed to step-down the output voltage.

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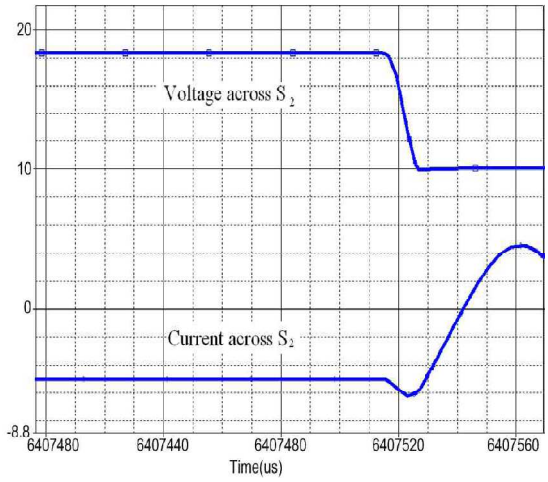
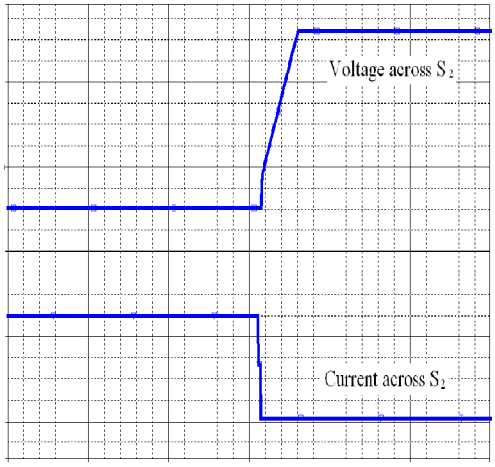
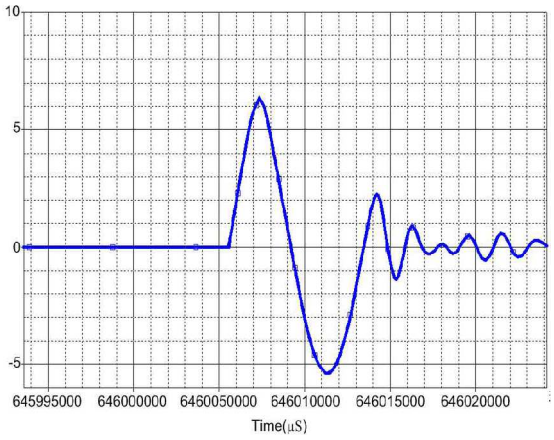
Simulation Results



(a)



(b)



(c)

Fig.6,7,8. Simulation results. a) Voltage and current across main switches S2 (S1 in active mode is short circuit) at turn-on time. b) Voltage and current across main switches S1, S2 at turn-off time. c) Current through Lr.(V: 100 V/div, I: 1 A/div, and Time: 5 ms/div).

Conclusion

A tri state dc-dc buck converter with a high conversion ratio is proposed. Such a converter can operate under a collateral input and output across their various strategy of inputs. The various form of duty cycles were performed under their modulated techniques. The response of the injection appears in the capacitor voltage according to the gain of the LCL filter. The BPF and the HPF are used to detect the only response from the injected component. The absolute value of the response through the and is averaged As a result, the deterioration fault of the filter-side capacitor is determined through the comparison between the experimental value and calculated value.

References

[1] H. M. Pirouzy and M. T. Bina, "Modular multilevel converter based STATCOM topology suitable for medium-voltage unbalanced systems," *Journal of Power Electronics*, Vol. 10, No. 5, pp. 572-578, Sep. 2010.

[2] E. Babaei, "Optimal topologies for cascaded sub-multilevel converters," *Journal of Power Electronics*, Vol.10. N0.3, pp-251-261..

[3] F. Iturriz and P. Ladoux, "Phase-controlled multilevel converters based on dual structure associations," *IEEE Trans. Power Electron.*, Vol. 15, No. 1, pp. 92-102, Jan. 2000.

[4] H. Mohammadi and M. T. Bina, "A transformerless medium-voltage STATCOM topology based on extended modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 26, No. 5, pp. 1534-1545, May 2011.

[5] M. L. Heldwein, S. A. Mussa, and I. Barbi, "Three-phase multilevel PWM rectifiers based on conventional bidirectional converters," *IEEE Trans. Power Electron.*, Vol. 25, No. 3, pp. 545-549, Mar. 2010.

[6] M. Hagiwara and H. Akagi, "Control and experiment of pulsewidth-modulated modular multilevel converters," *IEEE Trans. Power Electron.*, Vol. 24, No. 7, pp. 1737-1746, Jul. 2009.

[7] K. Hasegawa and H. Akagi, "A new DC-voltage-balancing circuit including a single coupled inductor for a five-level diode-clamped

ISSN: 2277-9655
Impact Factor: 1.852

PWM inverter," *IEEE Trans. Ind. Appl.*, Vol. 47, No. 2, pp. 841-852, Mar./Apr. 2011.

[8] Y. Zhang and L. Sun, "An efficient control strategy for a five-level inverter comprising flying-capacitor asymmetric h-bridge," *IEEE Trans. Ind. Electron.*, Vol. 58, No. 9, pp. 4000-4009, Sep. 2011.

[9] Z. Du, L. M. Tolbert, B. Ozpineci, and J. N. Chiasson, "Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter," *IEEE Trans. Power Electron.*, Vol. 24, No. 1, pp. 25-33, Jan. 2009.